intel®

APPLICATION NOTE

AP-361

October 1992

4

Implementing the Integrated Registers of the Series 2 Flash Memory Card

MARKUS LEVY
SENIOR TECHNICAL APPLICATIONS ENGINEER

Order Number: 292096-002

Implementing the Integrated Registers of the Series 2 Flash Memory Card

CONTENTS

CONTENTS

INTRODUCTION

Intel's first generation flash memory cards(1) forever changed the vision of solid-state storage. Electrically rewritable, non-volatile, reliable, yet economical in high densities, these cards provided a unique solution for the portable computing industry demanding such media. The second generation of flash memory cards provide even higher densities, lower power consumption and a higher level of functionality. The Series 2 Flash Memory Card delivers a major technology breakthrough by supporting densities up to 20 MBytes(2), an integrated memory control register set (**Component Management Registers** or **CMRs**) and PCMCIA 2.0/ExCA™ compliance.

Intel's 8-Megabit FlashFile™ Memory, 28F008SA, provides the foundation for the Series 2 Flash Memory Card. Its properties include data-write and block-erase automation, sixteen 64 KByte, separately-erasable blocks, a Ready/$\overline{busy}$ output pin, and a Powerdown mode. Within the Series 2 Card, high-functionality ASICs link the flash memory devices with the PCMCIA-specified electrical interface. These ASICs handle buffering, decoding and all control signals. They also contain the CMRs and hardwired Card Information Structure (CIS) used by system software to enhance device-level functions.

The OEM has many hardware and software alternatives for using the Series 2 Card. From a hardware perspective, the Intel 82365SL offers the most practical solution for controlling the PCMCIA socket in a PC solid-state drive application. This component, called the PC Card Interface Controller, provides the ExCA compliant hardware interface between the host system and the Series 2 Cards (and all other ExCA-compliant cards). As shown in Figure 1, the fundamental glue logic consists of a V_{PP} generator and V_{CC} control, a latching transceiver and address and decode signal buffers. Embedded systems not requiring an ExCA-compliant socket, can provide proper card signals with discrete circuitry.

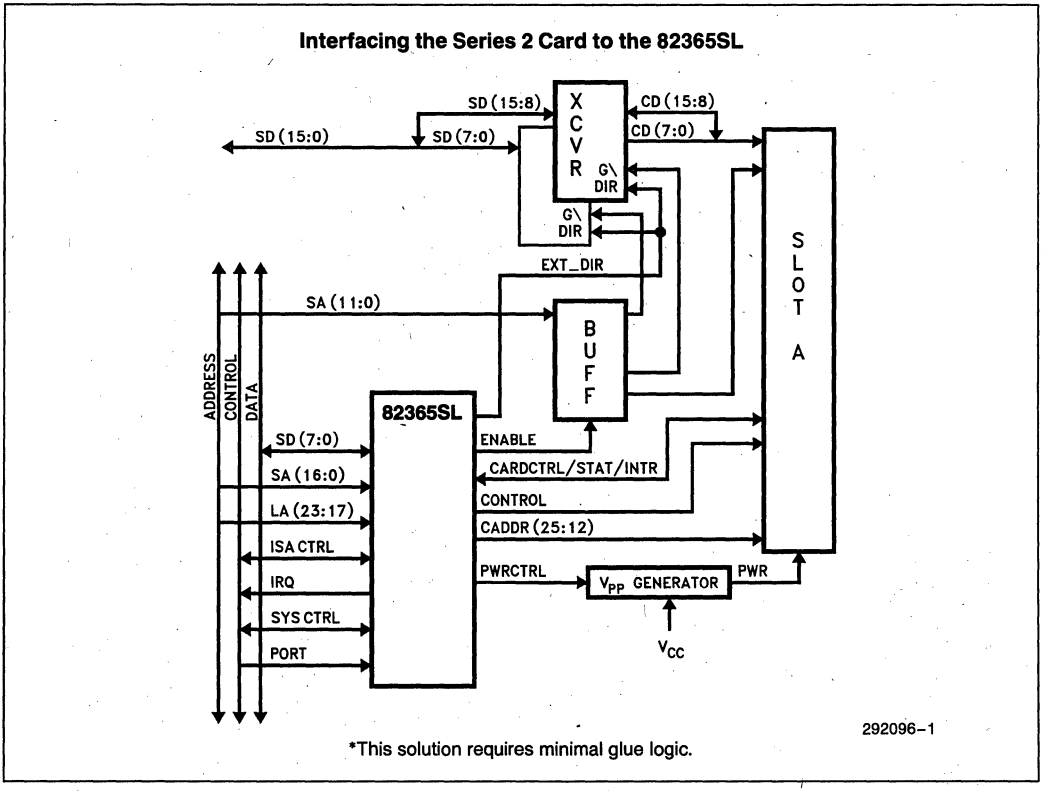


Figure 1. The 82365SL Establishes ExCA™ Compatibility with Minimal Glue Logic

NOTES:
1. The Bulk-Erase iMC001FLKA, iMC002FLKA, and iMC004FLKA (One, Two and Four Megabytes, respectively).
2. Higher density cards may be realized in the future as component densities go beyond 8 Megabits.

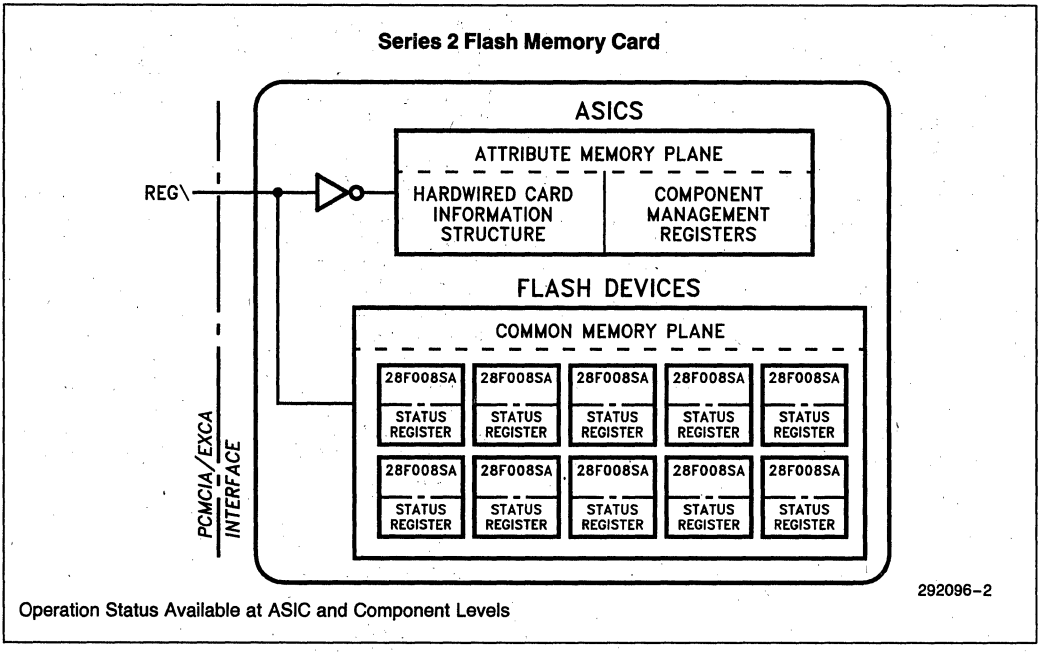


Figure 2. Selecting the Attribute or Common Memory Planes

Computer systems using the Series 2 Card as a solid-state disk drive employ file management software, such as Microsoft's* Flash File System with ExCA software. This software capitalizes on the architectural benefits of flash memory. It includes drivers that interface directly to the Series 2 Card. Beyond specifying the hardware architecture, ExCA provides a software solution that consists of modular software pieces designed for easy adaptation to the various hardware platforms and memory technologies. The various pieces of the ExCA system may be obtained from your BIOS vendor. Essentially, this means that a system OEM is relieved of having to implement the integrated registers of the Series 2 Flash Memory Card.

This application note supplements the information contained in the Series 2 Flash Memory Card Data Sheet. It benefits OEMs developing their own Series 2 Flash Memory Card software pieces, including custom flash file management software and software for embedded systems running non-DOS applications. Specifically, it describes the software aspects of implementing the card's CMRs which provide software control of many 28F008SA functions, elevating the system designer above device-level issues used by higher-level file system software.

SERIES 2 COMPONENT MANAGEMENT REGISTERS

The CMRs optimize the Series 2 Flash Memory Card's performance by supplying a software-controlled interface to the individual devices within the card. As shown in Figure 2, they are accessed as memory-mapped I/O in the Attribute Memory Plane by pulling the card's Register Select pin low ($\overline{REG}$, pin 61)(3). CMRs can be divided into two basic categories; those defined by the PCMCIA Release 2.0 specification and Intel defined "Performance Enhancement Registers".

PCMCIA RELEASE 2.0 DEFINED

Soft Reset Register
(Configuration Option Register)

During card operation, it may be necessary to place the card into a known state by resetting the 28F008SA-level Status Registers and the CMRs in the ASICs to their power-on conditions (Figure 3). Specifically, in the

NOTE:
3. No switch-over setup-time from Common Memory is needed when PCMCIA timing requirements are met.

Component Managment Registers[4]

Defined by the PCMCIA R2.0 specification
- **Soft Reset Register [5]—(R/W)**
- **Global Powerdown Register [6]—(R/W)**

PERFORMANCE ENHANCEMENT REGISTERS designed to deliver control benefits tied directly to the Intel 28F008SA:

- **Sleep Control Registers—(R/W)**
- **Ready-Busy Status Registers—(RO)**
- **Ready-Busy Mode Registers—(R/W)**
- **Ready-Busy Mask Registers—(R/W)**
- **Write Protection Registers—(R/W)**
- **Card Status Register—(RO)**

ASICs, this reset affects the PwrDwn bit (**Global Powerdown Register**), the **Sleep Control Register**, the **Ready-Busy Mode Register**, the **Ready-Busy Mask Register**, and the CISWP and CMWP bits (**Write Protection Register**). There are several ways to enter power-on status:

1. Issuing a hardware reset, with a complete system reset or socket reset through the interface hardware, affects the entire system or the Series 2 Card, respectively.
2. During normal operation of many portable systems, such as those employing the 386SL™ microprocessor, tremendous power savings are realized by entering a suspend state. In this state, power to the card's socket is removed. After reapplying power, the card automatically attains its power-on status. Therefore, before removing power from the Series 2 Card, system software must save the contents of the Component Management Registers. It should also be pointed out, that a startup period must elapse to allow all internal circuitry to stabilize before accessing the card. This time period depends on host system power supply capabilities.[7]
3. The third method utilizes a software-controlled mechanism built into the Series 2 Card. This option, activated with the **Soft Reset Register**, provides a simple approach for placing the card in its power-on state without time delay.

The **Soft Reset Register** (Figure 4) contains a soft reset (SRESET) bit that performs a function similar to the hardware reset invoked by the card's RESET pin ($\overline{RST}$, pin 58)[8]. Achieve the reset condition by issuing a two-step write sequence to the SRESET bit (i.e. toggling from 0 to 1 and back to 0).

During reset (SRESET = 1), the ASICs drive the flash memory array into the deep-sleep mode. This aborts any device operations in progress and resets each device's Status Register. After initiating a soft reset, the SRESET bit *must* be cleared (zero) to enable access to the flash memory array or write to another CMR. The host system can clear this bit by writing in a zero or issuing a hardware reset.

Power-On Conditions*

ALL DEVICES IN STANDBY MODE.
SOFTWARE WRITE-PROTECT DISABLED.
ALL DEVICES' READY/$\overline{BUSY}$ OUTPUTS UNMASKED.
PCMCIA-READY/$\overline{BUSY}$ MODE ENABLED.
READY/$\overline{BUSY}$ OUTPUT PIN GOES TO READY.

NOTE:
Generated by Hardware Reset or Toggling SRESET Bit.

Figure 3

NOTES:
4. R = READ, W = WRITE, RO = READ ONLY
5. Referred to as Configuration Option Register by PCMCIA R2.0.
6. Referred to as Configuration and Status Register by PCMCIA R2.0.
7. As specified by PCMCIA Release 2.0.
8. Soft reset puts all devices into power-down mode and requires a recovery time after returning from soft reset (500 ns for reads and 1 μs for writes).

Soft Reset Register
(Configuration Option Register)

PCMCIA-Defined

CIS ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4000H	SRESET	PCMCIA CONFIGURATION INDEX POWERS UP AND RESETS TO ZERO						

- Toggle SRESET to reset and return to standby-mode.
- For power-on default, SRESET = 0.

Figure 4. Useful for placing the card into a known state

The other two fields (not implemented with the Series 2 Card), defined in this register by the PCMCIA R2.0 specification, include the Configuration Index and the LevlREQ. After powerup or soft reset, the Configuration Index contains zeros to maintain compatibility as a Memory-Only Interface. The LevlREQ bit is hardwired to zero.

GLOBAL POWERDOWN REGISTER

PCMCIA R2.0 Defined

(Configuration and Status Register)

The portable system designer strives to minimize power consumption in every conceivable way. Solid-state storage devices using Intel Flash Memory deliver significant power consumption reductions (when compared to the mechanical disk) and therefore play an important part of the system design considerations. The portable system aimed at power conservation looks to shut down portions of system circuitry not in use (i.e. the solid-state drive not accessing files, the screen's backlight when the keyboard has not been touched in a certain amount of time, etc.). Powering down the entire socket achieves a minimal power usage status. However, the powerup recovery time from this approach produces varying delays.

The Series 2 Card offers the optimal solution with the **Global Powerdown Register** (Figure 5). Writing a one (1) to the Power-Down Bit (PwrDwn, bit 2) of this register puts all internal devices into the Deep-Sleep Mode by pulling every device's $\overline{PWD}$ input low[9]. In the Deep-Sleep mode, a 20 Megabyte Series 2 Card consumes 90% less current versus the standby mode current[10].

When the host system drives the two card enable pins high[11], the Series 2 ASIC circuitry blocks system-level address and data signals from the internal devices. Additionally, latching address buffers and data transceiv-

Global Powerdown Register
(Configuration Option Register)

PCMCIA-Defined

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4002H	ZEROS					PWRDWN	ZEROS	

- Powerdown places all devices into Deep-Sleep mode.
- Write zeros to maintain PCMCIA compatibility.
- PWRDWN = 0 after reset.

Figure 5

NOTES:
9. The remaining fields in this register (Changed, SigChg, IOis8, Audio, Intr and Rsvd) are tied low in the Series 2 Card for PCMCIA compatibility and for simplifying software masking.
10. I_{CCS} = 30 μA vs, I_{CCSL} = 0.2 μA; refer to 28F008SA Data Sheet. The ASICs consume 1 μA.
11. $\overline{CE1}$ (pin 7) and $\overline{CE2}$ (pin 42) = V_{IH}

SAMPLE 80X86 CODE TO HANDLE RECOVERY-PERIOD TIMING

```
   GLOBAL_PWD      EQU     4002H       ;Global PowerDown Register
   NOT_PWRDWN      EQU     0H

   MOV AX, MEM_CARD_BASE       ;Load card address
   MOV ES, AX
   MOV DI, GLOBAL_PWD          ;Pointer setup

;Software assumes already in REG# mode access
   MOV BYTE PTR ES:[DI], NOT_PWRDWN ;Clears PWRDWN bit

   MOV CX, RECOVERY_TIME       ;Based on speed of processor
 FOR_A_WHILE:
   LOOP FOR_A_WHILE
```

Figure 6. Assembly Language Code for Returning from "Deep-Sleep" Mode

ers on the host side eliminate address and data signal switching at the Series 2 Card input buffers further reducing power consumption levels. In other words, to achieve the lowest power consumption levels, these signals should not be floated or tristated.

After clearing the PwrDwn bit, the device-recovery times must be met before accessing the flash memory. As shown in Figure 6, the recovery period can be implemented using a simple software algorithm(12).

Prior to entering the Powerdown Mode, your software must check operation status for data-writes or block-erases in progress(13). Any operations in progress will be terminated when powering down the flash array. The 28F008SA does not maintain Status Register contents in the Powerdown Mode. Therefore, when the card returns to standby mode, all devices will report **successful** status (Status Register = 80H) indicating the need for software drivers to use the powerdown function intelligently.

PERFORMANCE ENCHANCEMENT REGISTERS

Sleep Control Register
(Performance Enhancement Register)

The powerdown functionality of the **Global Powerdown Register** has a global affect on all devices. In many solid-state storage applications, reading or writing files only requires access to select device pairs and the remaining devices could be kept in Deep-Sleep status until needed.

Sleep Control Registers
Performance Enhancement Register

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
411AH	RESERVED						DEVICES 18/19	DEVICES 16/17
4118H	DEVICES 14/15	DEVICES 12/13	DEVICES 10/11	DEVICES 8/9	DEVICES 6/7	DEVICES 4/5	DEVICES 2/3	DEVICES 0/1

- For reset, all devices powered up (bits = 0).
- On cards less than 20 megabytes, absent devices read as "0"s.
- Bits cleared to zero by SRESET and RESET.

Figure 7. Allows Selective Powerdown of Devices within the Series 2 Card

NOTE:
12. PCMCIA does not specify a maximum recovery time. Recovery times, varying for different card technologies, must be handled on a case-by-case basis.
13. Polling the individual device's Status Register, the Ready/Busy Status Register, or the RDY/$\overline{BSY}$ bit in the Card Status Register.

28F008SA Status Register Bit Definition

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WSM STATUS	ERASE SUSPEND STATUS	ERASE STATUS	WRITE STATUS	VPP STATUS	RESERVED		

Figure 8. Read during Write or Erase Operations to Determine Status

The **Sleep Control Register** (Figure 7) offers this option; each bit provides power down for a specific device pair. Except for the global vs individual affect, this register functions identically to the **Global Powerdown Register**. The global powerdown can be enabled while individual devices are sleeping. Disabling the global PWRDWN does not affect prior bit settings of the **Sleep Control Register**.

In many applications using the Series 2 Card, the card will be in the Standby Mode a large percentage of the time. This avoids device recovery times associated with complete socket power off or entering the Deep-Sleep Mode. In the Standby Mode, the **Sleep Control Register** offers the greatest advantage over the **Global Powerdown Register**. With the capability of controlling individual device pairs, a power savings improvement of approximately 16 times (based on typical current values) will be seen. This is derived from the following information:

- 28F008SA devices in Deep-Sleep; $I_{CC} = 0.2\ \mu A$, $I_{PP} = 0.1\ \mu A$.
- 28F008SA devices in Standby; $I_{CC} = 30\ \mu A$, $I_{PP} = 1\ \mu A$.
- ASICs in Standby and Sleep; $I_{CC} = 1\ \mu A$.
- With device-pair control, unaccessed devices remain in Deep Sleep.

Although the other operating modes (read, data-write, or block-erase) also experience power savings by using the **Sleep Control Register**, the effects are not as significant relative to the higher current requirements of those modes.

When using the **Sleep Control Register**, software must account for the same device-recovery time of the global powerdown method. To access files (or data) that span multiple device pairs (and experience uninterrupted access), software can perform a "look-ahead" function to determine which device pairs must be powered up.

READY-BUSY STATUS REGISTER

Performance Enhancement Register

The automated data-write and block-erase capability of the Intel 28F008SA FlashFile Memory results in a significant performance improvement. Furthermore, automation simplifies system-level interfacing as the user only delivers the proper command and monitors the operation's READY/BUSY status. Referring to the 28F008SA Data Sheet (or Figure 8), operation status can be obtained from the device's *Status Register* or RY/$\overline{BY}$ pin. The device's Status Register allows software polling for ready status in addition to write and erase status. The RY/$\overline{BY}$ pin can be used to generate an interrupt when making a busy to ready transition. Regardless of the method used for determining ready status, the Status Register should be read to determine whether an operation was successful.

In the Series 2 Card, where multiple devices are present and multiple simultaneous operations can occur, software polling each device's Status Register requires extra software and time. Furthermore, the PCMCIA interface only has one RDY/$\overline{BSY}$ pin which obviously prevents 20 devices from hooking their individual RY/$\overline{BY}$ out to the system. The ASICs within the card take these signals and feed them into the **$\overline{BUSY}$ Status Register** (Figure 9). This facilitates multiple device-pair operations by allowing an analysis of all devices simultaneously. After initiating the data-write and block-erase operations, the system can switch the card to the Attribute Memory Plane to access these registers. Alternatively, each device's RY/$\overline{BY}$ signal funnels into a single "wired or" signal that becomes the PCMCIA-RDY/$\overline{BSY}$ pin driving an interrupt or polled through an I/O port.

When performing single device pair operations, Ready/Busy status should be accessed directly from the Status Register of the flash memory devices for the following reasons: 1) A device's Status Register must be read anyway to determine the result of an operation; 2) This saves several instructions required to switch to the Attribute Memory Plane.

Ready-Busy Status Register
Performance Enhancement Register

CIS ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4134H	RESERVED				DEVICE 19	DEVICE 18	DEVICE 17	DEVICE 16
4132H	DEVICE 15	DEVICE 14	DEVICE 13	DEVICE 12	DEVICE 11	DEVICE 10	DEVICE 9	DEVICE 8
4130H	DEVICE 7	DEVICE 6	DEVICE 5	DEVICE 4	DEVICE 3	DEVICE 2	DEVICE 1	DEVICE 0

- Each bit corresponds to a device's RY/$\overline{BY}$ signal.
- Devices not present (i.e. < 20 Megabytes) return ready status.

Figure 9. Monitors Individual Device's RY/$\overline{BY}$ Pins

Example for Monitoring Ready/Busy Status

(Assume ES contains memory card base address)

```
RDY_BSY_STATUS      EQU 4130H ;Register address
DEVICE_0            EQU 01H   ;Settings in register for specific devices
DEVICE_1            EQU 02H
DEVICE_2            EQU 04H
DEVICE_3            EQU 08H
DEVICE_4            EQU 10H
DEVICE_5            EQU 20H

XOR AX, AX                          ;Zero AX Register
MOV DI, RDY_BSY_STATUS

;Insert code to start write operation in first 3 Device Pairs
;i.e. Devices 0, 1, 2, 3, 4, 5.

OR AX, DEVICE_0
OR AX, DEVICE_1
OR AX, DEVICE_2
OR AX, DEVICE_3
OR AX, DEVICE_4
OR AX, DEVICE_5

;Assume card already in REG mode.
TEST BYTE PTR ES:[DI], AX       ;Zero flag cleared when programming
                                ;devices are ready.
```

4

READY-BUSY MASK REGISTER Performance Enhancement Register

As described earlier, completion of a data-write or block-erase operation can be determined by attaching the card's RDY/BSY pin into a system interrupt. This frees the host system to perform alternate tasks after initiating an operation. In other words, device-level automation allows Series 2 Card operations to become background tasks.

Occasions exist where the interrupt generated from a device becoming ready produces unacceptable latency times. For instance, data-write operations, completing in only 10 μs, realize a performance penalty dealing with interrupt latencies longer than the write time itself. The data-write operations would achieve a higher level of performance by using software polling techniques[14]. On the other hand, block-erase operations typically require one second. Therefore, these operations perform well as background tasks because the interrupt latency constitutes a small fraction of the total time.

The above discussion implies that the system interrupt should be disabled for data-writes and enabled for block-erases. What if an application requires simultaneous writes and erases? The Series 2 Flash Memory Card handles this situation with its Ready-Busy Mask Register (Figure 10). Setting the appropriate mask bits in the Ready-Busy Mask Register blocks the corresponding device's RY/$\overline{BY}$ signals. With a device's mask bit set, the card's RDY/BSY pin and Card Status Register (bit 0) always reflect a ready condition, regardless of the operation status. Figure 11 displays a conceptual mask circuit for a single device. The mask settings have no effect on the card's Ready-Busy-Status Registers (providing direct access to each device's RY/$\overline{BY}$ output) or the Device Status Register. This allows software polling in the usual manner.

Ready-Busy Mask Register
Performance Enhancement Register

CIS ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4124H	RESERVED				DEVICE 19	DEVICE 18	DEVICE 17	DEVICE 16
4122H	DEVICE 15	DEVICE 14	DEVICE 13	DEVICE 12	DEVICE 11	DEVICE 10	DEVICE 9	DEVICE 8
4120H	DEVICE 7	DEVICE 6	DEVICE 5	DEVICE 4	DEVICE 3	DEVICE 2	DEVICE 1	DEVICE 0

1 = MASKED

Figure 10. Allows Masking of Individual Device's Ready/Busy Signals

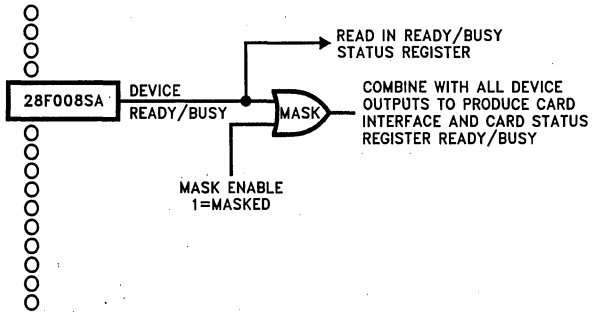
Selecting the Appropriate Device to Mask

Assume the register set DI:DX contains a 32-bit physical address into SERIES 2 card.
Each device pair represents 2 Megabytes (i.e. 200000H).

```
MOV CL, 5  ;Load shift count
SHR DI, CL ;Result in DI is device pair number to mask.

;Now determine whether to mask device pair for word operations or use Bit 0 of
the DX portion to determine high or low device (odd or even) for byte
operations.
```

NOTE:
14. Polling the individual device's Status Register, the Ready/Busy Status Register, or the RDY/BSY bit in the Card Status Register.



- Each device has a Ready/Busy (RY/$\overline{BY}$) output.
- When mask enabled, devices always appear ready.
- RY/$\overline{BY}$ available in RDY-BSY Status Register.

Figure 11. The Ready-Busy Mask is Very Useful for Write Optimization

READY-BUSY MODE REGISTER

Performance Enhancement Register

The PCMCIA specification for the Ready/Busy interface states that "*the RDY/$\overline{BSY}$ line is driven low by the memory card to indicate that the memory-card circuits are busy and unable to accept a data-transfer operation.*" Contrary to the PCMCIA specification, device-level data-write and block-erase automation enables the Series 2 Card to perform multiple operations simultaneously. Using the PCMCIA-specified method of RDY/$\overline{BSY}$ functionality for multiple device operations, the RDY/$\overline{BSY}$ interrupt does not notify the system until all devices finish because busy devices hold the RDY/$\overline{BSY}$ signal low, as shown in Figure 12. Multiple block erases (typical block erase time of 1 second) could present an unacceptable pushout if system software waits for the first available "clean" block to write data.

The Series 2 Card offers an alternative Ready/Busy mode (High-Performance Ready/Busy mode, alias "Levy"-mode) removing the performance impact of the PCMCIA mode. Circuitry internal to the ASIC catches every "READY-going" edge from each device. After an individual device becomes ready (Ready/Busy signal goes high), the system has the opportunity to immediately service the interrupt. System software must now toggle the CLEAR bit (bit 1) in the Ready-Busy Mode Register (Figure 14) to reactivate the Ready/Busy signal. Figure 13 demonstrates the resulting waveform.

The Series 2 Card powers up in the PCMCIA-mode. Switching into the High Performance mode requires a two step process, as shown in Figure 15. ASIC circuitry design prevents being able to write a zero to the RACK bit on the same cycle as entering the High-Performance RDY/BSY Mode. This intentional design technique eliminates the possibility of receiving a noise generated RDY/$\overline{BSY}$ rising edge, which would trigger an unwanted interrupt.

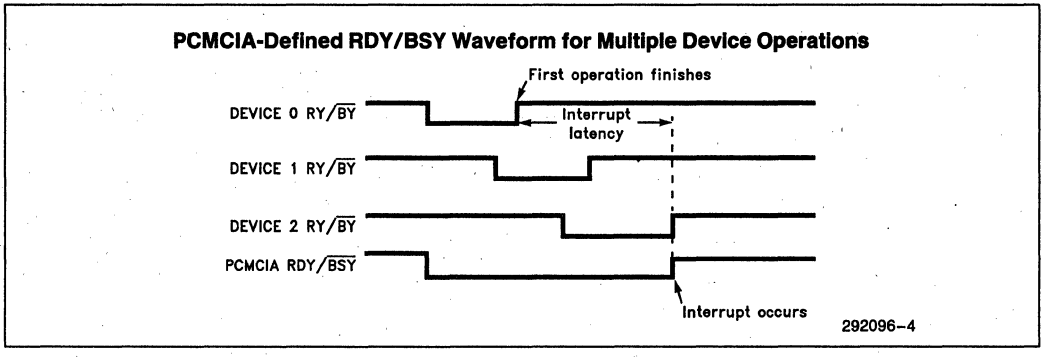
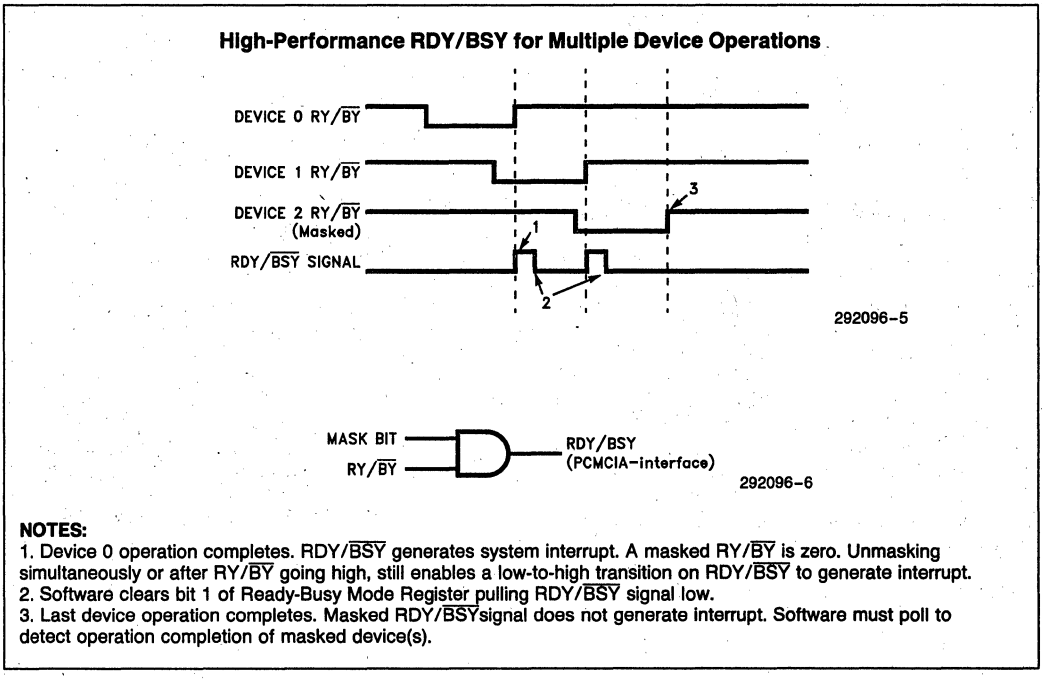


Figure 12. PCMCIA-Defined RDY/BSY Waveform for Multiple-Device Operations



NOTES:
1. Device 0 operation completes. RDY/$\overline{BSY}$ generates system interrupt. A masked RY/$\overline{BY}$ is zero. Unmasking simultaneously or after RY/$\overline{BY}$ going high, still enables a low-to-high transition on RDY/$\overline{BSY}$ to generate interrupt.
2. Software clears bit 1 of Ready-Busy Mode Register pulling RDY/$\overline{BSY}$ signal low.
3. Last device operation completes. Masked RDY/$\overline{BSY}$signal does not generate interrupt. Software must poll to detect operation completion of masked device(s).

Figure 13. High-Performance Mode Catches Each Device Going Ready

Ready/Busy Mode Register
Performance Enhancement Register

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4140H	RESERVED						RACK	MODE

- Mode = Ready/Busy Mode
  0 = PCMCIA Mode
  1 = High-Performance Mode
- RACK = Ready Acknowledge Bit
  Clear this bit after receiving ready status to prepare for next device's ready transition
- Register defaults to PCMCIA Mode for power on or reset. In PCMCIA Mode, RACK is a Don't Care

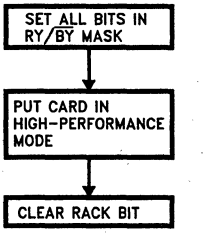
Figure 14. To Prevent Accidental Ready Transitions, a Three Step Sequence must be Followed to Enter High-Performance Mode

As discussed in the previous section, the block-erase operation benefits from the interrupt capabilities of the RDY/$\overline{BSY}$ signal. However, if your software only erases one device pair at any time, the PCMCIA-RDY/$\overline{BSY}$ Mode will be sufficient for two reasons: 1) Both devices started simultaneously will complete the erase operation almost at the same time; 2) in 16-bit access mode, both devices of the pair must be erased before writing.

To block-erase in multiple devices:

1. Be sure to mask all devices (in Ready/Busy Mask Register).
2. If not already done, place the Series 2 Card in the High-Performance Mode (refer to Figure 15).
3. Issue the block-erase command sequence to the appropriate devices.

Enabling High-Performance Ready/Busy Mode



Prevents ready devices from triggering an unwanted rising edge, and generating an interrupt after clearing RACK bit.

Write a one (1) to the Mode bit of the RY/BY Mode Register.

Write a zero (0) to the RACK bit of the RY/BY Mode Register. The hardware requires this sequence to eliminate unwanted interrupts caused by signal-bounce.

Figure 15. Entering High-Performance Mode

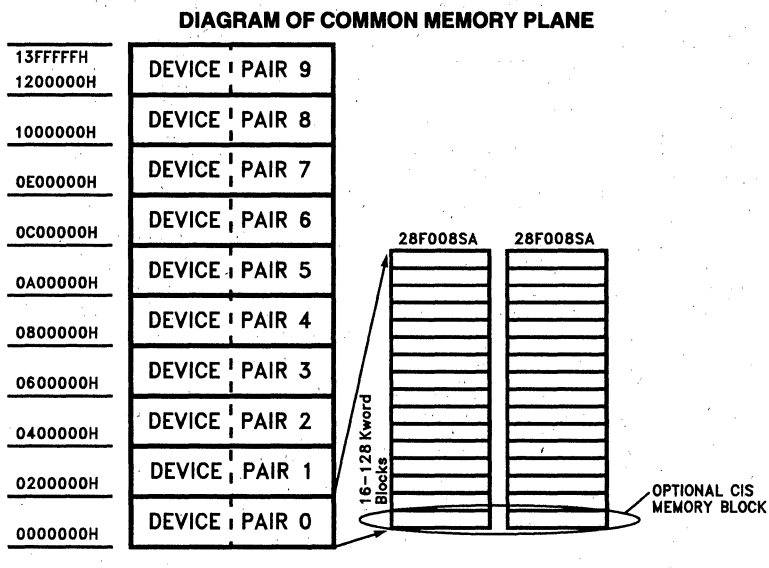
4. Unmask appropriate **Ready-Busy Mask Register** bits. The circuitry catches devices with already completed erase operations with the conceptual setup shown in Figure 13. Use a RAM-based variable or register for an erase-block queue to monitor erasing devices.

The interrupt service routine (ISR) can be as simple as removing the erase block from the queue. It could also be used to notify the system that this block is free to use. Regardless of the ISR implementation, it should include the following basic procedures:

1. Set all RY/BY masks in the **Ready-Busy Mask Register**. This prevents additional interrupts within the ISR (i.e. prevent re-entrant interrupt). Keep track of mask setup to reinstate before ISR exit.
2. Check the queue of erasing devices and read the Ready-Busy Status Register to determine which device completed the operation.
3. Service the erased block(s). Even though one erased block generated the interrupt, more blocks may have completed erasing at this point.
4. Clear RACK in the Ready-Busy Mode Register.
5. Before exiting the ISR, reset the mask. This "catches" devices that went ready during the ISR and will cause a re-entrant ISR. However, at this point in the ISR, this will not affect system or software integrity.

WRITE-PROTECTION REGISTER

The Series 2 Card contains a PCMCIA-defined, hardwired Card Information Structure (CIS) accessed in the Attribute Memory Plane. This data structure provides fundamental, unchanging information pertaining to the card. It includes card size, type of components, access speed, etc. Situations exist where the user needs to include custom-format information, such as card partitioning and operating system specific information.



- The first block pair of the first device pair is the common memory CIS; write protect using CISWP bit of Write Protection Register.
- Write protect the remaining 159 block pairs using the CMWP bit of the Write Protection Register.

Figure 16. The WRITE PROTECT REGISTER Blocks Writes to the Two Sections of the Common Memory Plane

This information can be loaded in the Common Memory CIS during card format (refer to Figure 16). Typically, once this information is written, it would rarely change. The Series 2 Card provides a means of locking this area of memory, as well as the remainder of the Common Memory array with the **Write Protection Register** (Figure 17). The **Write Protection Register** has an advantage over the mechanical write protect switch in that it allows software to control user write access to the card's data (the mechanical switch can be easily switched off enabling card writes). For example, a pen-based system may use this feature to protect its read-only operating system stored within the Series 2 Card.

The CIS Write Protect Bit (CISWP, bit 0) prevents writes to the Common Memory CIS blocks. When software determines that this block of memory contains valid, *custom-format* information (contains PCMCIA tuple data structure), the CISWP Bit could be set to prevent accidental data corruption by another application. Note that if an End-User format utility is provided, this software must be careful not to destroy the custom format information which could be accessed if the CISWP Bit was deactivated. The Common Memory Write Protect Bit (CMWP, bit 1) prevents writes to the remainder of the Common Memory Plane (i.e. minus the Common Memory CIS blocks). To "software"-write-protect the *entire* Common Memory Plane, both bits must be set.

Write Protection Register
Performance Enhancement Register

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4104H	RESERVED						CMWP	CISWP

- CISWP = Common Memory CIS Write Protect
- CMWP = Common Memory Write Protect
- "1" = Write Protected

Figure 17. Provides a Software Implementation of the Write Protect Switch

CARD STATUS REGISTER

Performance Enhancement Register

This (Read-Only) register provides quick access to generalized conditions within the Series 2 Card (Figure 18). It provides a shorthand method for checking the following functions:

- Ready/Busy Status
- Ready/Busy Masking
- Deep-Sleep Modes
- Setting of Mechanical Write-Protect Switch
- Software Write Protect Status
- Soft Reset Status

Where the RY/$\overline{BY}$ Bit (bit 0, **Card Status Register**) displays the operation status of the cumulative devices within the card, the **Ready-Busy Status Registers** reflects the status of each individual device. Bit 0 (RDY/$\overline{BSY}$) mirrors the card's RDY/$\overline{BSY}$ (Ready/Busy) output pin, also reflecting any Ready/Busy masking conditions. Two circumstances warrant the use of this bit: 1) When the hardware interrupt triggered by the RDY/$\overline{BSY}$ pin produces an unacceptably long latency period, this bit should be software polled instead to increase performance; 2) When multiple devices have data-write/block-erase operations in progress, reading this cumulative Ready/Busy status will be quicker than reading multiple status registers within each device. However, when the application requires immediate access to each device as it finishes an operation, individual Device Status Registers or the card's **Ready-Busy Status Register** must be used.

Card Status Register
Performance Enhancement Register

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4100H	ADM	ADS	SRESET	CMWP	PWRDWN	CISWP	WP	RDY/$\overline{BSY}$

- RDY/$\overline{BSY}$ = Reflects PCMCIA interface RDY/BSY pin, 0 = busy
- WP = Mechanical Write Protect Switch, 0 = off
- CISWP = Common Memory CIS Write Protect, 0 = off
- PWRDWN = Powerdown Reflects PWRDWN in Global Power Down Reg, 1 = Power Off
- CMWP = Common Mode Write Protect, 0 = Off
- SRESET = Soft Reset Reflects SRESET in SOFT RESET Reg, 1 = Soft Reset
- ADS = Any Device Pair Powered Down, OR'd Condition of Sleep Control Reg, 1 = Power Off
- ADM = Any Device Masked, OR'd Condition of Ready-Busy Mask Reg, 1 = Masked

Figure 18. Provides Generalized Card and Device Information

Bit 1 reflects the card's mechanical switch position (1 = Write Protected). This switch disables any writes to the card. Two software strategies can be implemented for this bit: 1) Assume the card's Write-Protect switch is off. Attempt to write to the card and only check the Write-Protect status if the data-write fails (which it will if the switch is on); 2) Check the switch first to avoid the possibility of failing a data-write. The choice depends on the application. For a solid-state disk continuously updating files, the former is more appropriate because the Write-Protect switch will probably be off.

Bits 2 (CISWP = Common Memory CIS) and 4 (CMWP = Common Memory Write Protect) are direct (Read Only) inputs from the **Write-Protect Register**. These bits should be checked in a manner similar to that for Bit 1 (WP). For more detail refer to the **Write-Protection Register** section.

The PwrDwn Bit (bit 3) provides a (Read Only) version of the PwrDwn Bit in the **Global Powerdown Register** (1 = PwrDwn). Only the Attribute Memory Plane is available with the Powerdown feature enabled, allowing access to the **Component Management Registers**.

The SRESET Bit (bit 5) provides a (Read-Only) version of the SRESET Bit in the **Soft Reset Register** (1 = Locked in soft reset state).

SUMMARY

The Series 2 Flash Memory Card delivers the hardware capabilities required for implementing a solid-state storage device. Software engineers will find the features of this card both flexible and powerful when coupled with flash-optimized filing systems, such as Flash File System from Microsoft. This application note has discussed the various methods of using the **Component Management Registers** to facilitate designs incorporating the SERIES 2 card.

- PCMCIA-Defined Registers provide generalized assistance for memory card interfacing.
- Performance Enhancement Registers boost software control over the card's internal flash memory devices.

GLOSSARY

Attribute Plane: Memory plane within the card selected by pulling the $\overline{REG}$ pin low. This random access memory contains the CIS and Component Management Registers.

Block-Erase: Erasing sections of a single flash memory device.

Bulk-Erase: Erasing the entire flash device simultaneously.

Common Memory: The memory card's main memory array.

Common Memory-Card Information Structure: The first block pair of the first device pair. Useful for storing custom format information, such as partitioning of the card.

Component Management Registers (CMR): Memory-mapped I/O registers used to control device-level functions.

Deep-Sleep Mode: A special very low power mode useful for saving power when not accessing the flash memory components.

Device-Pair: Arrangement of the 8-bit 28F008SA devices in the SERIES 2 card in a word-wide manner.

ExCA: System Implementation (hardware and software) of PCMCIA R2.0.

Hardwired Card Information Structure (CIS): Embedded into the Attribute Memory Plane to describe non-changing information about the SERIES 2 Card (i.e. density, speed).

Levy Mode: alias for the High-Performance mode for Ready/Busy notification.

Personal Computer Memory Card International Association (PCMCIA): The organization formed to promote interchangeability of IC cards by providing a standardized mechanical, electrical and metaformat interface.

Performance Enhancement Registers: Memory-Mapped I/O registers included by Intel in the Series 2 Card to boost performance by providing software control of the internal 28F008SA functions.

Ready/Busy: Indicator used to determine when a data-write or block-erase operation has completed. Symbolized by RY/$\overline{BY}$ for the 28F008SA and RSY/$\overline{BSY}$ at the Series 2 Card interface.

Status Register: A register internal to a 28F008SA FlashFile™ Memory device used to determine write and erase operation status.

RELATED DOCUMENTS

28F008SA, 8 Megabit, FlashFile™ Memory Data Sheet
Series 2 Flash Memory Card Data Sheet
82365SL, PC Card Interface Controller Data Sheet
PCMCIA PC Card Standard Release 2.0
Exchangeable Card Architecture Specification

4